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JC893 U.S. PTO 12/28/01

PTO/SB/05 (03-01)
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JC679 U.S. PTO 10/034458 12/28/01

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	CU-2797 VE
First Inventor	Gyo Un CHOI et al
Title	A LIQUID CRYSTAL DISPLAY FOR TESTING DEFECTS OF WIRING IN PANE
Express Mail Label No.	L 698183704

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. [X] Fee Transmittal Form (e.g., PTO/SB/17) *(Submit an original and a duplicate for fee processing)*
2. [ ] Applicant claims small entity status. See 37 CFR 1.27.
3. [X] Specification [Total Pages 17]
   (preferred arrangement set forth below)
   - Descriptive title of the invention
   - Cross Reference to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to sequence listing, a table, or a computer program listing appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
4. [X] Drawing(s) *(35 U.S.C. 113)* [Total Sheets 7]
5. Oath or Declaration [Total Pages 5]
   a. [X] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 CFR 1.63 (d)) *(for continuation/divisional with Box 18 completed)*
      i. [ ] DELETION OF INVENTOR(S)
      Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1 63(d)(2) and 1 33(b)
6. [ ] Application Data Sheet. See 37 CFR 1.76
7. [ ] CD-ROM or CD-R in duplicate, large table or Computer Program *(Appendix)*
8. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer Readable Form (CRF)
   b. Specification Sequence Listing on:
      i. [ ] CD-ROM or CD-R (2 copies); or
      ii. [ ] paper
   c. [ ] Statements verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

9. [X] Assignment Papers (cover sheet & document(s))
10. [ ] 37 CFR 3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
11. [ ] English Translation Document *(if applicable)*
12. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
13. [ ] Preliminary Amendment
14. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
15. [X] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. [ ] Nonpublication Request under 35 U.S.C. 122 (b)(2)(B)(i). Applicant must attach form PTO/SB/35 or its equivalent.
17. [ ] Other: .....

18. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below and in a preliminary amendment, or in an Application Data Sheet under 37 CFR 1.76:*

[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No.: _____/_____

Prior application information. Examiner _____ *Group Art Unit:* _____

For CONTINUATION OR DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 5b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

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Address					
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Country		Telephone		Fax	

Name (Print/Type)	Vangelis Economou	Registration No. (Attorney/Agent)	32341
Signature	Vangelis Economou	Date	12/28/01

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FEE TRANSMITTAL for FY 2002

Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 780.00

Complete if Known	
Application Number	
Filing Date	
First Named Inventor	Gyo Un CHOI et al
Examiner Name	
Group Art Unit	
Attorney Docket No.	CU-2797 VE

METHOD OF PAYMENT *(check all that apply)*

☒ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☐ Deposit Account:

Deposit Account Number: 12-0400

Deposit Account Name: Ladas & Parry

The Commissioner is authorized to: *(check all that apply)*

☐ Charge fee(s) indicated below ☒ Credit any overpayments

☒ Charge any additional fee(s) during the pendency of this application

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FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	740	201	370	Utility filing fee	740.
106	330	206	165	Design filing fee	
107	510	207	255	Plant filing fee	
108	740	208	370	Reissue filing fee	
114	160	214	80	Provisional filing fee	

SUBTOTAL (1) ($) 740.

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

	Extra Claims		Fee from below	Fee Paid
Total Claims	12 -20** =	0	X	=
Independent Claims	3 - 3** =	0	X	=
Multiple Dependent				=

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	84	202	42	Independent claims in excess of 3
104	280	204	140	Multiple dependent claim, if not paid
109	84	209	42	** Reissue independent claims over original patent
110	18	210	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0.

***or number previously paid, if greater; For Reissues, see above*

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for *ex parte* reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	400	216	200	Extension for reply within second month	
117	920	217	460	Extension for reply within third month	
118	1,440	218	720	Extension for reply within fourth month	
128	1,960	228	980	Extension for reply within fifth month	
119	320	219	160	Notice of Appeal	
120	320	220	160	Filing a brief in support of an appeal	
121	280	221	140	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,280	241	640	Petition to revive - unintentional	
142	1,280	242	640	Utility issue fee (or reissue)	
143	460	243	230	Design issue fee	
144	620	244	310	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Processing fee under 37 CFR 1.17(q)	
126	180	126	180	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	40.
146	740	246	370	Filing a submission after final rejection (37 CFR § 1.129(a))	
149	740	249	370	For each additional invention to be examined (37 CFR § 1.129(b))	
179	740	279	370	Request for Continued Examination (RCE)	
169	900	169	900	Request for expedited examination of a design application	

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 40.

SUBMITTED BY

Name (Print/Type)	Vangelis Economou	Registration No. (Attorney/Agent)	32341	Telephone	(312)427-1300
Signature	Vangelis Economou			Date	12/28/01

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A LIQUID CRYSTAL DISPLAY FOR TESTING DEFECTS OF WIRING IN PANEL

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to a liquid crystal display and, more particularly, to a liquid crystal display capable of testing defects of wiring in panel.

2. Description of the Prior Art

Figs. 1A to 1C are drawings showing a Module structure of conventional liquid crystal display.

As shown in the drawings, Fig. 1A comprises a X-PCB 2 for supplying graphic signals to a panel 1, a Y-PCB 4 for applying TFT driving signals and a FPC 7 for connecting the PCBs.

And, Fig. 1B shows a structure that the FPC 7 is removed and Fig. 1C shows that the Y-PCB 4 is removed and signals for driving gate driver integrated circuit IC are

applied through wiring in the panel 1.

Here, panels of each module have different shapes and wiring for driving gate driver IC is formed on the upper part of array substrate of panel.

Fig. 2 is a drawing showing a conventional method of panel test. Referring to Fig. 2, odd lines of data lines (D1, D2 …Dn) are connected to data odd pad 17a and even lines of the data lines (D1, D2…Dn) are connected to data even pad 17b. In the same method, gate lines (G1, G2…Gn) are connected to gate odd pad 15a and gate even pad 15b. And, Vcom pad 13 is connected to all pixels of TFT array 11 on panel and wiring 20 is formed on the corner of upper part of panel 10.

Then, signals are applied to five resulting pads in order to test whether a unit pixel is normally operated or not. That is, it is possible to test short of line and pixel by applying voltage to the gate odd pad 15a, the gate even pad 15b, the data odd pad 17a, the data even pad 17b and the Vcom pad 13.

However, the conventional liquid crystal display has a disadvantage that it is difficult to test disconnection and

short by wiring formed on the upper part of panel and additional device is required to test defects of wiring.

SUMMARY OF THE INVENTION

Therefore, the present invention has been made to solve the above problems and an object of the present invention is to provide a liquid crystal display for testing defects of wiring in panel capable of testing disconnection and short of wiring in panel when signals are applied by connecting data line or gate line or common voltage line in panel to each pad through wiring formed on the outside of panel in a zigzag shape.

In order to accomplish the above object, the present invention comprises: a TFT array unit comprising a plurality of gate lines and data lines formed in a matrix shape, having TFT transistors at the intersection of the gate line and the data line; a data pad unit commonly connected to the plurality of data lines, receiving signals for driving the data line; and a wiring unit for testing defects of data line connected between the data pad unit and the data line, testing disconnection and short of the data line.

The data pad unit comprises a first data pad unit commonly connected to the odd data line of the plurality of data lines, receiving signals for driving the odd data line and a second data pad unit commonly connected to even data line of the plurality of data lines, receiving signals for driving the even data line.

The wiring unit for testing defects of data line comprises a first wiring unit for testing defects of data line connected between the first data pad unit and the odd data, testing disconnection and short of the odd data line and a second wiring unit for testing defects of data line connected between the second data pad unit and the even data line, testing disconnection and short of the even data line.

The first and the second wiring units for testing defects of data line are formed in a zigzag shape.

According to another embodiment of the present invention, a liquid crystal display for testing defects of wiring in panel comprises: a TFT array unit comprising a plurality of gate lines and data lines formed in a matrix shape, having TFT transistors at the intersection of the gate lines and the data lines; a gate pad unit commonly connected to the

plurality of gate lines, receiving signals for driving the gate line; and a wiring unit for testing defects of gate line connected between the gate pad unit and the gate line, testing disconnection and short of the gate line.

The gate pad unit comprises a first gate pad unit commonly connected to odd gate line of the plurality of gate lines, receiving signals for driving the odd gate line and a second gate pad unit commonly connected to even gate line of the plurality of gate lines, receiving signals for driving the even gate line.

The wiring unit for testing defects of gate line comprises a first wiring unit for testing defects of first gate line connected between the first gate pad unit and the odd gate line, testing disconnection and short of the odd gate line and a second wiring unit for testing defects of second gate line connected between the second gate pad and the even gate line, testing disconnection and short of the even gate line.

The first and the second wiring units for testing defects of gate lines are formed in a zigzag shape.

According to still another embodiment of the present invention, a liquid crystal display comprises: a TFT array unit comprising a plurality of gate lines and data lines formed in a matrix shape, having a TFT transistors on each pixel at the intersection of the gate line and the data line; a common voltage pad unit for applying common voltage to common voltage line connected to each pixel; and a wiring unit for testing defects of common voltage line connected between the common voltage line and the common voltage pad unit, testing disconnection and short of the common voltage line.

The common voltage pad unit comprises a first common voltage pad unit commonly connected to odd common voltage line of the plurality of common voltage lines, receiving signals for driving the odd common voltage line and a second common voltage pad unit commonly connected to even common voltage line of the plurality of common voltage lines, receiving signals for driving the even common voltage line.

The wiring unit for testing defects of common voltage line comprises a first wiring unit for testing defects of common voltage line, connected between the first common voltage pad unit and the odd common voltage line, testing

disconnection and short of the odd common voltage line and a second wiring unit for testing defects of common voltage line, connected between the second common voltage pad unit and the even common voltage line, testing disconnection and short of the even common voltage line.

The first and the second wiring units for testing defects of common voltage line are formed in a zigzag shape.

According to the present invention, it is possible to test defects of wiring in panel by a conventional panel test method, thereby improving reliability of panel.

BREIF DESCRIPTION OF THE DRAWINGS

Figs. 1A to 1C are drawings showing module structure of general liquid crystal display.

Fig. 2 is a drawing showing a conventional panel test method.

Figs. 3A and 3B are block diagrams showing a liquid crystal display for testing defects of wiring in panel according to the present invention.

Figs. 4A and 4B are drawings showing a method of testing disconnection and short of wiring in panel according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

The above objects, and other features and advantages of the present invention will become more apparent after reading the following detailed description when taken in conjunction with the appended drawings.

Figs. 3A and 3B are drawings showing a method of testing wiring in panel according to the present invention.

Referring to Fig. 3A, a TFT array unit 11 in panel 10 is arranged with a plurality of gate lines $G_1, G_2 \ldots G_n$ and data lines $D_1, D_2 \ldots D_n$ from the TFT array unit. The odd lines of the gate lines $G_1, G_2 \ldots G_n$ are connected to a gate odd pad 15a and the even lines are connected to a gate even pad 15b. The data lines $D_1, D_2 \ldots D_n$ are connected to a data odd pad 17a and a data even pad 17b. The zigzag connection wiring 30a on the upper part of panel 10 is connected to a first line D1 of the data odd pad 17a in series.

Referring to Fig. 3B, a test structure is formed in the same method as that in Fig. 3A. However, wiring is formed in a separated zigzag connection wiring 30b and then, connected to a first line D_1 of data odd pad 17a and a first line D_2 of data even pad 17b in series. Therefore, it is possible to test disconnection and short of wiring by applying signal for the test to data odd pad 17a and data even pad 17b. When short is generated, TFT of data even line 17b, whereto signal is not applied, is also operated as well as data odd line 17a.

Figs. 4A and 4B are drawings showing a method of testing disconnection and short of wiring in panel according to the present invention.

Referring to Fig. 4A, when disconnection is generated between wiring of panel, the disconnected wiring is connected to a first line D_1 of data odd pad 17a. Therefore, when signal is applied to the data odd pad 17a, TFT of the disconnected first line D_1 is not operated and TFTs of other lines $D_3, D_5 \ldots$ are normally operated.

Fig. 4B shows a method of testing defects when short is generated between wiring in panel. Referring to Fig. 4B, the

data odd pad 17a is connected to wiring connected to data even pad 17b. Therefore, when signal is applied to data odd pad 17a, TFT of second data line D_2 is operated as well as TFT of the first data line D_1. If the two are operated at the same time, it is determined that short defects are generated.

Although it is not shown in the drawings, it is possible to test defects by connecting the same method to gate odd pad 15a and gate even pad 15b and by connecting the zigzag wiring 30a to the common voltage Vcom pad 13 in series.

As described above, according to the present invention, it is possible to test defects of wiring in panel by connecting wiring in a zigzag shape or by separating and connecting wiring in a zigzag shape and then, connecting the resultant to the gate pad unit, the data pad unit and the common voltage pad unit.

And, according to the present invention, it is possible to remove Flexible Printed Circuit FPC or Printed Circuit Board PCB, thereby reducing manufacturing cost and the size of product.

Although the preferred embodiment of this invention has

been disclosed for illustrative purpose, those skilled in the art will appreciate that various modifications, alterations, additions and substitutions are possible, without departing from the scope and spirit of the invention.

WHAT IS CLAIMED IS

1. A liquid crystal display for testing defects of wiring in panel, comprising:

a TFT array unit comprising a plurality of gate lines and data lines formed in a matrix shape, having TFT transistors at the intersection of the gate line and the data line;

a data pad unit commonly connected to the plurality of data lines, receiving signals for driving the data lines; and

a wiring unit for testing defects of data line, connected between the data pad unit and the data line, testing disconnection and short of the data line.

2. The liquid crystal display according to claim 1, wherein the data pad unit comprising a first data pad unit commonly connected between odd data lines of the plurality of data lines, receiving signals for driving the odd data lines and a second data pad unit commonly connected between even data lines of the plurality of data lines, receiving signals for driving the even data line.

3. The liquid crystal display according to claim 2, wherein the wiring unit for testing defects of data line comprises a first wiring unit for testing defects of data line connected between the first data pad unit and the odd data line, testing disconnection and short of the odd data line and a second wiring unit for testing defects of data line connected between the second data pd unit and the even data line, testing disconnection and short of the even data line.

4. The liquid crystal display according to claim 3, wherein the first and the second wiring units for testing defects of data line are formed in a zigzag shape.

5. The liquid crystal display for testing defects of wiring in panel comprising:

a TFT array unit comprising a plurality of gate lines and data lines formed in a matrix shape, having TFT transistors at the intersection of the gate line and the data line;

a gate pad unit commonly connected between the plurality of gate lines, receiving signals for driving the gate line; and

a wiring unit for testing defects of gate line

connected between the gate pad unit and the gate line, testing disconnection and short of the gate line.

6. The liquid crystal display according to claim 5, wherein the gate pad unit comprises a first gate pad unit commonly connected between odd gate lines of the plurality of gate lines, receiving signals for driving the odd gate line and a second gate pad unit commonly connected between even gate lines of the plurality of gate lines, receiving signals for driving the even gate line.

7. The liquid crystal display according to claim 6, wherein the wiring unit for testing defects of gate line comprises a first wiring unit for testing defects of gate line connected between the first gate pad unit and the odd gate line, testing disconnection and short of the odd gate line and a second wiring unit for testing defects of gate line connected between the second gate pad unit and the even gate line, testing disconnection and short of the even gate line.

8. The liquid crystal display according to claim 7, wherein the first and the second wiring units for testing defects of gate line are formed in a zigzag shape.

9. A liquid crystal display for testing defects of wiring in panel comprising:

a TFT array unit comprising a plurality of gate lines and data lines formed in a matrix shape, having TFT transistors in each pixel at the intersection of the gate line and the data line;

a common voltage pad unit for applying common voltage to common voltage line connected to each pixel; and

a wiring unit for testing defects of common voltage line connected between the common voltage line and the common voltage pad unit, testing disconnection and short of the common voltage line.

10. The liquid crystal display according to claim 9, wherein the common voltage pad unit comprises a first common voltage pad unit commonly connected between odd common voltage line of the plurality of common voltage lines, receiving signals for driving the odd common voltage line and a second common voltage pad unit commonly connected between even common voltage lines of the plurality of common voltage lines, receiving signals for driving the even common voltage line.

11. The liquid crystal display according to claim 10, wherein the wiring unit for testing defects of common voltage line comprises a first wiring unit for testing defects of common voltage line connected between the first common voltage pad unit and the odd common voltage line, testing disconnection and short of the odd common voltage line and a second wiring unit for testing defects of common voltage line connected between the second common voltage pad unit and the even common voltage line, testing disconnection and short of the even common voltage line.

12. The liquid crystal display according to claim 11, wherein the first and the second wiring units for testing defects of common voltage line are formed in a zigzag shape.

ABSTRACT OF THE DISCLOSURE

A liquid crystal display capable of testing defects of wiring in panel. The liquid crystal display comprising: a TFT array unit comprising a plurality of gate lines and data lines formed in a matrix shape, having TFT transistors at the intersection of the gate line and the data line; a data pad unit commonly connected to the plurality of data lines, receiving signals for driving the data lines; and a wiring unit for testing defects of data line, connected between the data pad unit and the data line, testing disconnection and short of the data line.

FIG. 1A
(PRIOR ART)

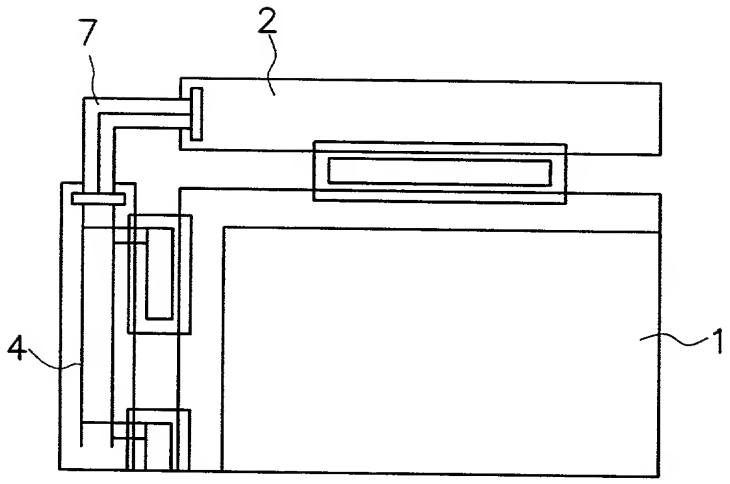


FIG. 1B
(PRIOR ART)

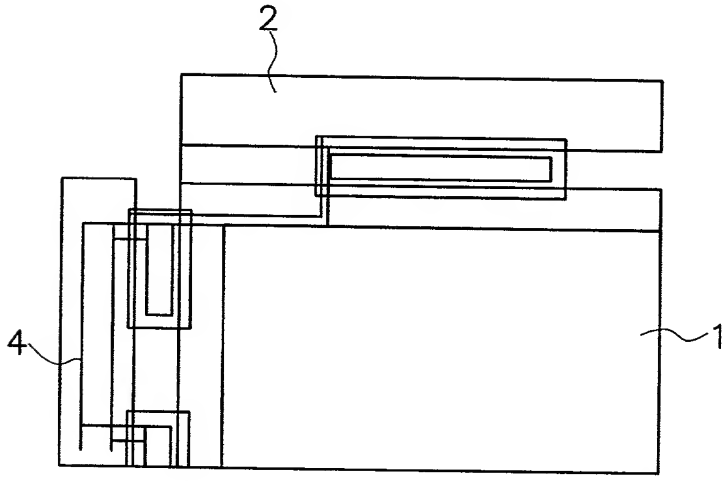


FIG. 1C
(PRIOR ART)

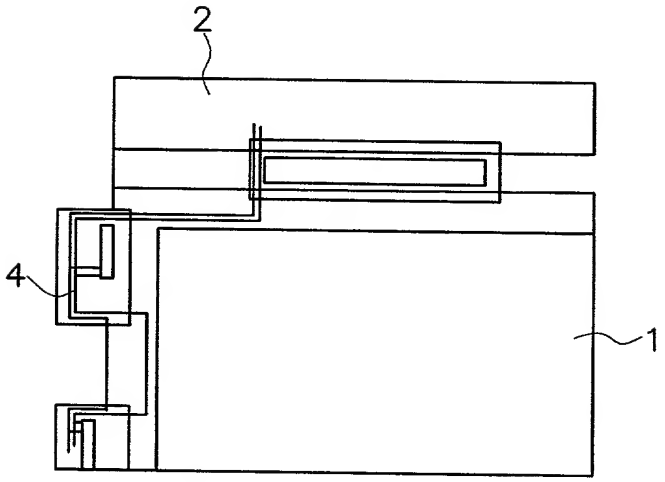


FIG.2

(PRIOR ART)

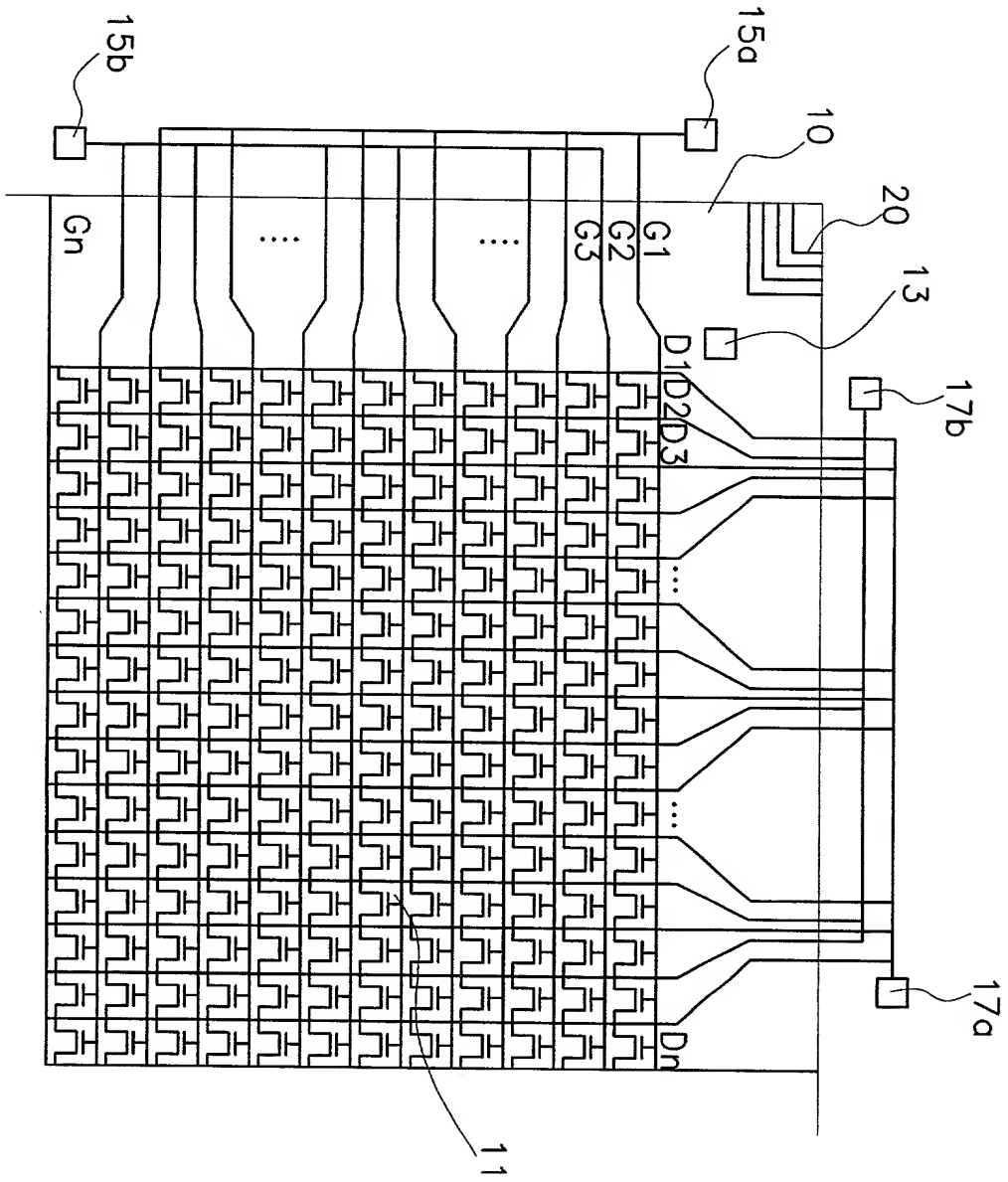


FIG.3A

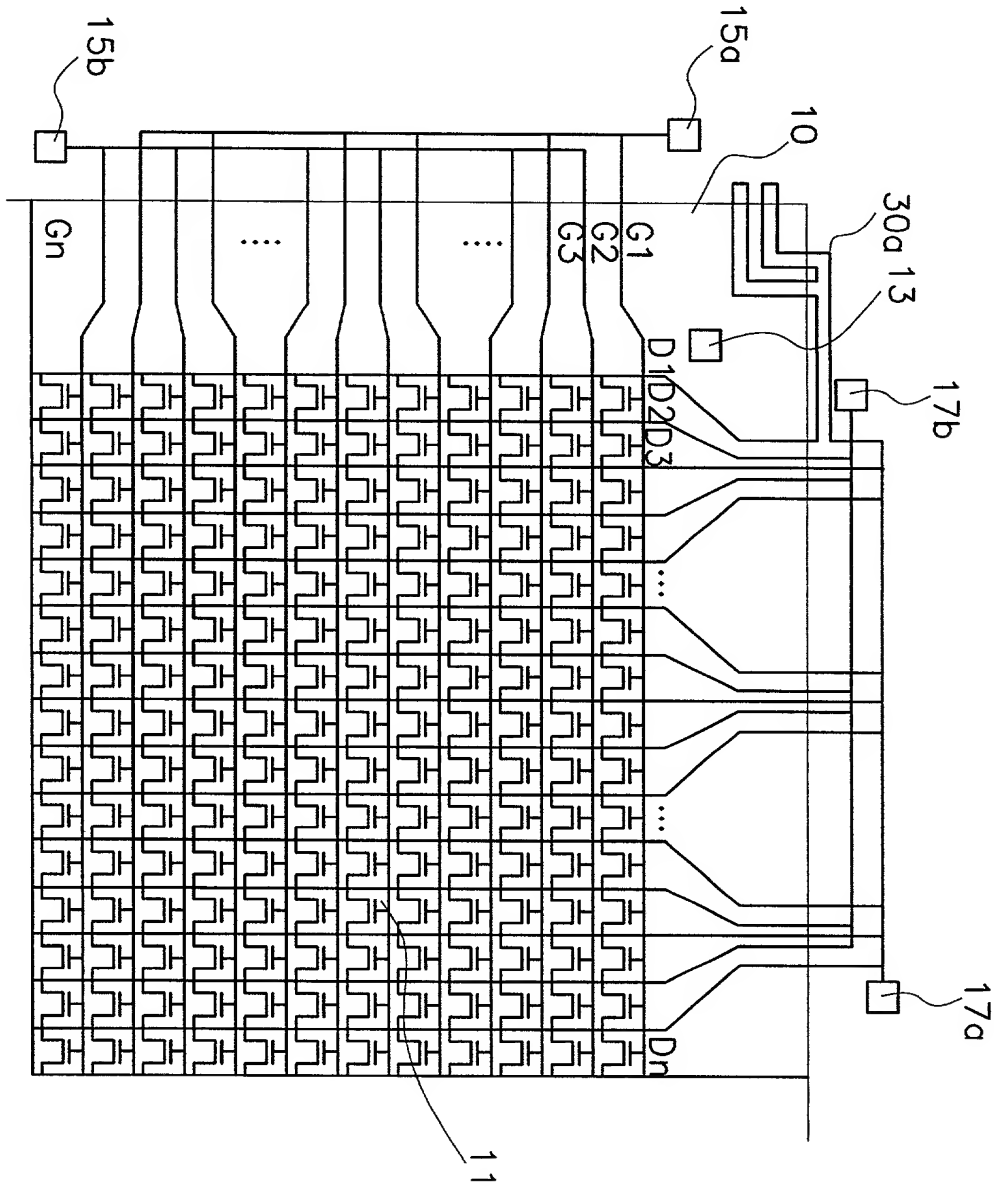


FIG.3B

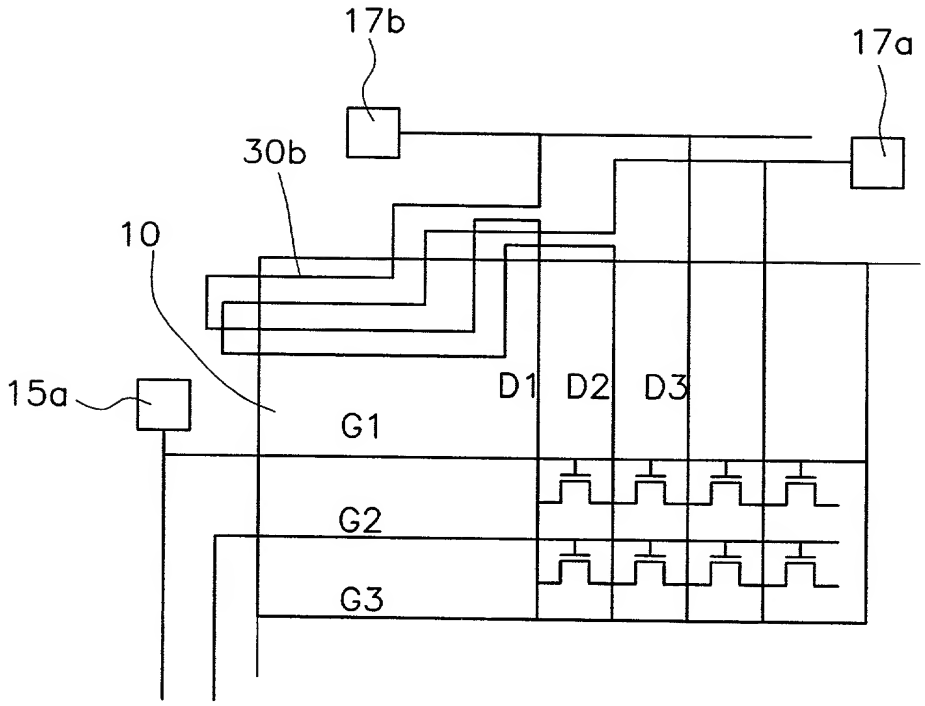


FIG.4A

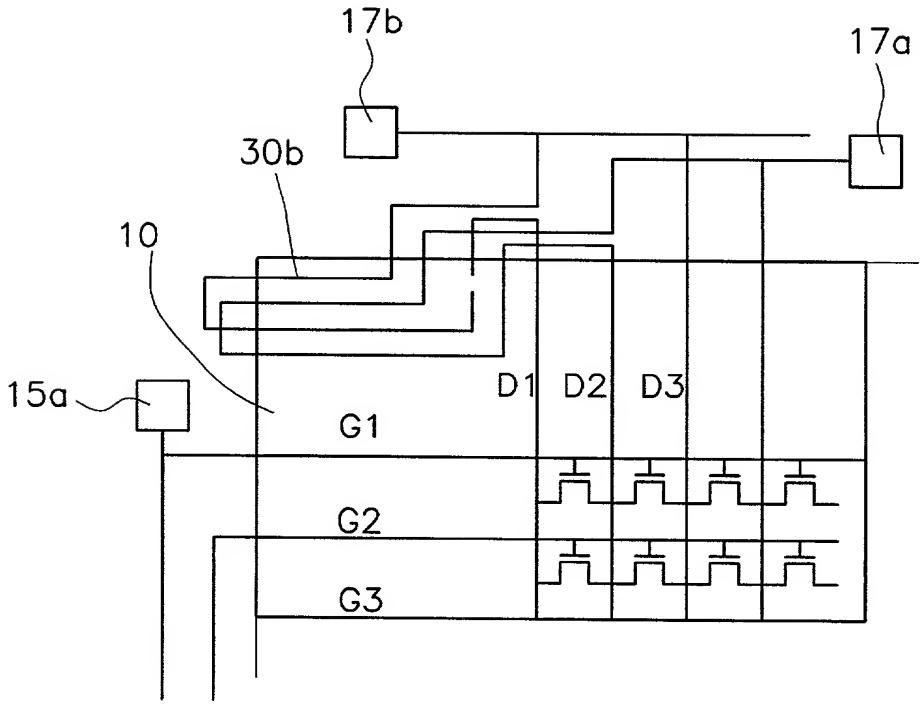
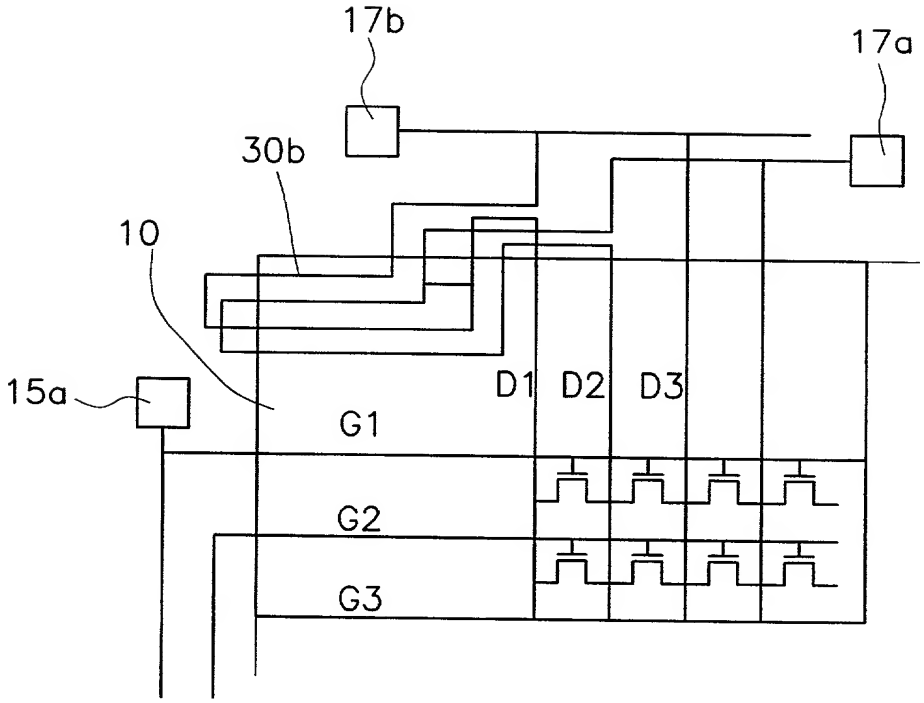


FIG.4B



L 698 183704

PATENT

Docket:

COMBINED DECLARATION AND POWER OF ATTORNEY

(ORIGINAL, DESIGN, NATIONAL STAGE OF PCT, SUPPLEMENTAL, DIVISIONAL, CONTINUATION OR CIP)

As a below named inventor, I hereby declare that:

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- [ ] design
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- [ ] national stage of PCT

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- [ ] divisional
- [ ] continuation
- [ ] continuation-in-part (CIP)

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WARNING: If the inventors are each not the inventors of all the claims, an explanation of the facts, including the ownership of all the claims at the time the last claimed invention was made, should be submitted.

My residence, post office address and citizenship are as stated below, next to my name. I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter that is claimed, and for which a patent is sought on the invention entitled:

TITLE OF INVENTION

A LIQUID CRYSTAL DISPLAY FOR TESTING DEFECTS OF WIRING IN PANEL

SPECIFICATION IDENTIFICATION

the specification of which: *(complete (a), (b) or (c))*

☒ (a) is attached hereto.

☐ (b) was filed on _____ as ☐ Serial No. _____ or
☐ Express Mail No. *(as Serial No. not yet known)* _____
and was amended on _____ *(if applicable).*

Note: Amendments filed after the original papers are deposited with the PTO that contain new matter are not accorded a filing date by being referred to in the Declaration. Accordingly, the amendments involved are those filed with the application papers or, in the case of a supplemental Declaration, are those amendments claiming matter not encompassed in the original statement of invention or claims. See 37 CFR 1.67.

☐ (c) was described and claimed in PCT International Application No. _____ filed on _____ and as amended under PCT Article 19 on _____ *(if any).*

ACKNOWLEDGEMENT OF REVIEW OF PAPERS AND DUTY OF CANDOR

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information, which is material to patentability as defined in 37, Code of Federal Regulations, § 1.56,

(also check the following items, if desired)

☐ and which is material to the examination of this application, namely, information where there is a substantial likelihood that a reasonable Examiner would consider it important in deciding whether to allow the application to issue as a patent, and

☐ in compliance with this duty, there is attached an information disclosure statement, in accordance with 37 CFR 1.98.

PRIORITY CLAIM (35 U.S.C. º 119(a)-(d))

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed.

(complete (d) or (e))

☐ (d) no such applications have been filed.

☒ (e) such applications have been filed as follows.

Note: Where item (c) is entered above and the international application which designated the U.S. itself claimed priority check item (e), enter the details below and make the priority claim.

PRIOR FOREIGN/PCT APPLICATION(S) FILED WITHIN 12 MONTHS
(6 MONTHS FOR DESIGN) PRIOR TO THIS APPLICATION
AND ANY PRIORITY CLAIMS UNDER 35 U.S.C. º 119(a)-(d)

COUNTRY (OR INDICATE IF PCT	APPLICATION NUMBER	DATE OF FILING (day/month/year)	PRIORITY CLAIMED UNDER 35 USC 119
Republic of Korea	2000-87509	30/12/2000	☒ YES NO ☐
			☐ YES NO ☐

CLAIM FOR BENEFIT OF PRIOR U.S. PROVISIONAL APPLICATION(S)
(35 U.S.C. º 119(e))

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

PROVISIONAL APPLICATION NUMBER	FILING DATE

ALL FOREIGN APPLICATION(S), IF ANY, FILED MORE THAN 12 MONTHS
(6 MONTHS FOR DESIGN) PRIOR TO THIS U.S. APPLICATION

_____

_____

Note: If the application filed more than 12 months from the filing date of this application is a PCT filing forming the basis for this application entering the United States as (1) the national stage or (2) a continuation, divisional, or continuation-in-part, then also complete ADDED PAGES TO COMBINED DECLARATION AND POWER OF ATTORNEY FOR DIVISIONAL, CONTINUATION OR CIP APPLICATION for benefit of the prior U.S. or PCT application(s) under 35 U.S.C. § 120.

POWER OF ATTORNEY

I hereby appoint the following practitioner(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith *(list name and registration number)*.

Thomas F. Peterson, 24790; Richard J. Streit, 25765; Donald P. Reynolds, 26220; W. Dennis Drehkoff, 27193; Vangelis Economou, 32341; Brian W. Hameder, 45613; Valerie Neymeyer-Tynkov, Reg. 46956; Paul B. West, 18947; Joseph H. Handelman, 26179; Peter D. Galloway 27885; John Richards, 31503; Iain C. Baillie, 24090; Richard P. Berg, 28145

☐ Attached, as part of this declaration and power of attorney, is the authorization of the above-named practitioner(s) to accept and follow instructions from my representative(s).

SEND CORRESPONDENCE TO:

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DECLARATION

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

SIGNATURE(S)

Note: Carefully indicate the family (or last) name, as it should appear on the filing receipt and all other documents.

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Residence

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Full name of fifth joint inventor, if any

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Inventor's signature

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Residence

Post Office Address